**Claims**

What is claimed is:

1. A finite impulse response filter cell, having at least three inputs and at least two outputs, the finite impulse response filter cell coupled to receive a clocking signal, comprising:

a multiplexer having at least two multiplexer inputs and an output, the multiplexer operable at substantially half the clocking signal rate, each of the at least two multiplexer inputs coupled to one of the at least three inputs of the finite impulse response filter cell;

a multiplier including an output and at least two multiplier inputs, the first multiplier input receiving a coefficient signal representing a FIR coefficient, the second multiplier input coupled to one of the at least three inputs of the finite impulse response filter cell;

a summer having at least two summer inputs and an output, the first and second summer inputs coupled to receive the multiplexer output and the multiplier output; and

at least two slave sample and hold circuits each having a slave input and a slave output, the at least two slave inputs of the plurality coupled to the summer output, the at least two slave outputs couple to form the at least two outputs of the finite impulse response filter cell, each slave sample and hold circuit operable at substantially half the clocking signal rate.

2. The finite impulse response filter of claim 1, wherein each coefficient signal comprises a digital value.

3. The finite impulse response filter of claim 1 further comprises a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

4. A finite impulse response filter cell, having at least two inputs and an output, the finite impulse response filter cell coupled to receive a clocking signal, comprising:

a multiplier including an output and at least two multiplier inputs, the first multiplier input receiving a coefficient signal representing a FIR coefficient, the second multiplier input coupled to one of the at least two inputs of the finite impulse response filter cell;

a summer having at least two summer inputs and an output, the first summer input coupled to receive the multiplier output, the second summer input coupled to one of the at least two inputs of the finite impulse response filter cell;

at least two slave sample and hold circuits each having a slave input and a slave output, the at least two slave inputs coupled to the summer output, each slave sample and hold circuit operable at half the clocking signal rate; and

a multiplexer having at least two multiplexer inputs and an output, each of the at least two slave outputs coupled to one of the at least two multiplexer inputs, the multiplexer operable at half the clocking signal rate, the multiplexer output couples to form the output of the finite impulse response filter cell.

5. The finite impulse response filter of claim 4, wherein each coefficient signal comprises a digital value.

6. The finite impulse response filter of claim 4, further comprises a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

7. A finite impulse response filter having an input and an output, comprising:

a master sample and hold circuit including a master input and a master output, the master input coupled to form the input of the finite impulse response

filter, the master sample and hold circuit operable to sample a first input signal and hold the value of the first input signal on the master output for a first predetermined period of time, the master sample and hold circuit operable at a clock speed;

at least two slave sample and hold circuits, each of the at least two slave sample and hold circuits comprising a slave input and a slave output, each the at least two slave inputs coupled to the master output, each of the at least two sample and hold circuits operable to sample the master output signal and hold the value of the signal on the plurality of slave outputs for a second predetermined period of time, the at least two slave sample and hold circuits operable at substantially *1/k* times the clock speed of the master sample and hold circuit, where *k* equals the number of slave sample and hold circuits;

a first multiplexer, having at least two first multiplexer inputs and a first multiplexer output, each of the at least two first multiplexer inputs coupled to one of the at least two slave outputs, the first multiplexer operable at substantially *1/k* times the clock speed of the master sample and hold circuit; and

at least one tap block having a tap block input and a tap block output, the tap block input coupled to the first multiplexer output, the at least one tap block, comprising,

a multiplier having a first and a second multiplier input and an multiplier output, the first multiplier input coupled to the tap block input, the second multiplier input coupled to receive a coefficient signal representing a FIR coefficient,

a summer including an output and a first and a second summer input, the first input coupled to the multiplier output,

at least two slave sample and hold circuits, each of the at least two slave sample and hold circuits comprising a slave input and a slave output, each the at least two slave inputs coupled to the summer output, the at least two slave sample and hold circuits operable at substantially *1/k* times the clock speed of the master sample and hold circuit, where *k* equals the number of slave sample and hold circuits,

a second multiplexer, having at least two second multiplexer inputs and a second multiplexer output, each of the at least two second multiplexer inputs coupled to one of the at least two slave outputs of the tap block, the second multiplexer operable at substantially *1/k* times the clock speed of the master sample and hold circuit, the second multiplexer output coupled to form the tap block output, the tap block output couples to form a filter output.

8. The finite impulse response filter of claim 7, wherein each coefficient signal comprises a digital value.

9. The finite impulse response filter of claim 7, further comprises a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

10. An finite impulse response filter having an output, comprising:

a master sample and hold circuit including a master input and a master output, the master input coupled to the input of the finite impulse response filter, the master sample and hold circuit operable to sample a first input signal and hold the value of the first input signal on the master output for a first predetermined period of time, the master sample and hold circuit operable at a clock speed;

a plurality of slave sample and hold circuits, each of the plurality of slave sample and hold circuits comprising a slave input and a slave output, each of the plurality of sample and hold circuits operable to sample a signal and hold the value of the signal on the plurality of slave outputs for a second predetermined period of time, the plurality of slave sample and hold circuits operable at substantially half the clock speed of the master sample and hold circuit;

a first pair of the plurality of slave sample and hold circuits having each slave input directly connected to the master output;

a plurality of multiplexers, each comprising at least a first and second multiplexer input and an multiplexer output, the first multiplexer operable at substantially half times the clock speed of the master sample and hold circuit, each first and second multiplexer inputs coupled to one pair of slave outputs;

a plurality of multipliers, each of the plurality of multipliers including an output and a first and a second multiplier input, each first multiplier input receiving a coefficient signal representing a FIR coefficient, each second multiplier input coupled to the output of the first multiplexer of the plurality of multiplexers; and

a plurality of summers, each of the summers including an output and a first and a second summer input, each first summer input coupled to one of the plurality of multiplier outputs, the second summer input of the first summer couples to ground, each remaining second summer inputs coupled to one of the plurality of multiplexer outputs, each pair of slave inputs succeeding the first pair of slave inputs connected to one of the plurality of summer outputs;

the number of plurality of slave sample and hold circuits equals 2N, the number of plurality of multiplexers equals N, the number of plurality of summers equals N, the number of plurality of multipliers N+2;

the multiplexer output of the last one of the plurality of multiplexers couples to form the output of the finite impulse response filter.

11. The finite impulse response filter of claim 10, wherein each coefficient signal comprises a digital value.

12. The finite impulse response filter of claim 10, further comprises a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

13. A method of making an finite impulse response filter which has an output, comprising the steps of:

coupling an input signal to a master input of a master sample and hold circuit;

directly connecting a master output of the master sample and hold circuit to a plurality of slave sample and hold circuits;

multiplexing the plurality of slave sample and hold circuit output signals;

directly connecting the multiplexed output to at least one tap block cell having a first and second input and an output, including a multiplier, a summer, a plurality of slave sample and hold circuits and a multiplexer;

supplying a fixed tap coefficient signal to an input of the multiplier;

multiplying the first input of the tap block cell and the fixed tap coefficient signal;

summing an output of the multiplier with the second input of the tap block cell;

connecting an output of the summer to the inputs of the plurality of slave sample and hold inputs of the tap block cell;

connecting the slave outputs of the plurality of slave sample and hold circuits to the plurality of multiplexer inputs of the multiplexer in the tap block; and

multiplexing the slave output signals to generate the finite impulse response filter output.

14. The method of claim 13, wherein the first input of the first tap block cell is grounded.